CLAIMS

What is claimed is:

1. A method for forming a semiconductor device structure comprising:

providing a semiconductor substrate assembly having a surface; and

Sub B1

forming a diffusion barrier layer over at least a portion of the surface, wherein the diffusion barrier layer comprises $RuSi_xO_y$.

Sub A1

2. The method of claim 1, wherein forming a diffusion barrier over at least a portion of the surface comprises forming a layer of $RuSi_xO_y$ where x is in the range of about 0.01 to about 10.

3. The method of claim 2, wherein forming a diffusion barrier over at least a portion of the surface comprises forming a layer of $RuSi_xO_y$ where x is about 0.4.

4. The method of claim 1, wherein forming a diffusion barrier over at least a portion of the surface comprises forming a layer of $RuSi_xO_y$ where y is in the range of about 0.01 to about 10.

5. The method of claim 4, wherein forming a diffusion barrier over at least a portion of the surface comprises forming a layer of $RuSi_xO_y$ where y is about 0.05.

6. The method of claim 1, wherein forming the barrier layer includes depositing $RuSi_xO_y$ by chemical vapor deposition.

7. The method of claim 1, wherein forming the barrier layer includes depositing $RuSi_xO_y$ by atomic layer deposition.

8. The method of claim 7, wherein forming the barrier layer includes depositing three to five monolayers of $RuSi_xO_y$.

Sub a17

9. The method of claim 1, wherein forming the barrier layer includes depositing $RuSi_xO_y$ by physical vapor deposition.

10. The method of claim 1, wherein forming said diffusion barrier layer comprises:

forming a layer of ruthenium relative to a silicon containing region; and

performing an anneal in an oxidizing atmosphere to form $RuSi_xO_y$ from the layer of ruthenium and the silicon containing region.

Sub B2

11. The method of claim 10, wherein forming the layer of ruthenium includes depositing the layer of ruthenium by chemical vapor deposition.

12. The method of claim 10, wherein forming the layer of ruthenium includes depositing the layer of ruthenium by atomic layer deposition.

13. The method of claim 12, wherein forming the layer of ruthenium includes depositing three to five monolayers of $RuSi_xO_y$.

Sub a21

14. The method of claim 10, wherein performing an anneal in an oxidizing atmosphere includes performing an anneal in an atmosphere including an oxidizing gas.

15. The method of claim 1, wherein the method further includes forming at least one additional conductive material over the diffusion barrier layer, and selecting the at least one additional conductive material from a group of a metal and a conductive metal oxide.

Sub a2

16. The method of claim 10, wherein performing the anneal to form said $RuSi_xO_y$ includes performing an anneal at a temperature in the range of about 400° C to about 1000° C.

17. The method of claim 10, wherein performing an anneal in an oxidizing atmosphere to form $RuSi_xO_y$ from the layer of ruthenium and the silicon containing region comprises performing said anneal in an atmosphere comprising air, oxygen, and oxygen-containing compounds.

18. The method of claim 10, wherein said silicon containing region includes at least a portion of said semiconductor substrate.

19. The method of claim 1, wherein forming said diffusion barrier layer comprises forming a diffusion barrier layer in an oxidizing atmosphere. B

Sub a3

20. The method of claim 19, wherein forming a diffusion barrier layer in an oxidizing atmosphere comprises forming a diffusion barrier layer in an atmosphere including an oxidizing gas.

21. A method for forming a capacitor comprising:

forming a first electrode on a portion of a substrate assembly;

forming a high dielectric constant material over at least a portion of the first electrode; and

forming a second electrode over the high dielectric constant material, wherein at least one of the first and second electrodes comprises a barrier layer formed of $RuSi_xO_y$, where x and y are in the range of about 0.01 to about 10.

22. The method of claim 21, wherein x and y are in the range of about 0.01 to about 1.

23. The method of claim 22, wherein x is about 0.4.

24. The method of claim 22, wherein y is about 0.05.

25. The method of claim 21, wherein the barrier layer is formed by chemical vapor deposition.

26. The method of claim 21,wherein the barrier layer is formed by atomic layer deposition.

27. The method of claim 21, wherein forming the barrier layer includes depositing three to five monolayers of $RuSi_xO_y$.

sub a4

28. A method for forming a capacitor comprising:

providing a silicon containing region of a substrate assembly;

forming a first electrode on at least a portion of the silicon containing region of the substrate assembly, the first electrode comprising a barrier layer of $RuSi_xO_y$, where x and y are in the range of about 0.01 to about 10;

providing a high dielectric constant material over at least a portion of the first electrode; and

providing a second electrode over the high dielectric constant material.

29. The method of claim 28, wherein x and y are in the range of about 0.01 to about 1.

30. The method of claim 28, wherein forming the barrier layer includes: forming a layer of ruthenium on the at least a portion of the silicon containing region; and annealing the layer of ruthenium formed on the at least a portion of the silicon containing region resulting in the $RuSi_xO_y$ barrier layer.

31. The method of claim 30, wherein forming the layer of ruthenium includes depositing the layer of ruthenium by chemical vapor deposition to a thickness of about 10Å to about 5000Å.

32. The method of claim 30, wherein forming the layer of ruthenium includes depositing the layer of ruthenium by atomic layer deposition to a thickness of about 10Å to about 5000Å.

33. The method of claim 32, wherein forming the layer of ruthenium includes depositing three to five monolayers of ruthenium.

34. The method of claim 31, wherein forming the layer of ruthenium comprises forming a layer of ruthenium to a thickness of about 50Å to about 500Å.

35. The method of claim 34, wherein forming the layer of ruthenium comprises forming a layer of ruthenium to a thickness of about 300Å.

36. The method of claim 28, wherein annealing the layer of ruthenium formed on the at least a portion of the silicon containing region includes annealing at a temperature in the range of about 400° C to about 1000° C for about 0.5 minutes to about 60 minutes in an inert gas atmosphere.

37. The method of claim 28, wherein the $RuSi_xO_y$ barrier layer is formed by chemical vapor deposition using a ruthenium precursor and a silicon precursor.

38. A method for forming a capacitor comprising:

providing a silicon containing region of a substrate assembly;

forming a first electrode on at least a portion of the silicon containing region of the substrate assembly, the forming of the first electrode comprising:

forming a barrier layer of $RuSi_xO_y$, where x and y are in the range of about 0.01 to about 10, and

forming one or more conductive layers relative to the $RuSi_xO_y$ barrier layer, the one or more conductive layers formed of at least one of a metal or a conductive metal oxide;

providing a high dielectric constant material over at least a portion of the first electrode; and

providing a second electrode over the high dielectric material.

39. The method of claim 38, wherein the one or more conductive layers are formed from materials selected from the group of RuO_2, RhO_2, MoO_2, IrO_2, Ru, Rh, Pd, Pt, Ir, W, WN, TaN, Os and OsO_2.

40. The method of claim 38, wherein forming the barrier layer includes:

forming a layer of ruthenium on the at least a portion of the silicon containing region; and

annealing the layer of ruthenium formed on the at least a portion of the silicon containing region resulting in the $RuSi_xO_y$ barrier layer.

41. The method of claim 38, wherein the $RuSi_xO_y$ barrier layer is formed by chemical vapor deposition using a ruthenium precursor and a silicon precursor.

42. The method of claim 38, wherein the $RuSi_xO_y$ barrier layer is formed by atomic layer deposition using a ruthenium precursor and a silicon precursor.

cont'd

43. The method of claim 42, wherein three to five layers of $RuSi_xO_y$ are formed.

Sub a8

44. A semiconductor device structure comprising:

a substrate assembly including a surface; and

a diffusion barrier layer over at least a portion of the surface, wherein the diffusion barrier layer is formed of $RuSi_xO_y$, where x and y are in the range of about 0.01 to about 10.

45. The structure of claim 44, wherein x and y are in the range of about 0.1 to about 1.

46. The structure of claim 45, wherein x is about 0.4.

47. The structure of claim 45, wherein y is about 0.03.

cont'd

48. The structure of claim 44, wherein the at least a portion of the surface is a silicon containing surface and further wherein the structure includes one or more additional conductive layers over the diffusion barrier layer formed of at least one of a metal and a conductive metal oxide.

Sub a9

49. The structure of claim 48, wherein the one or more conductive layers are formed from materials selected from the group consisting of RuO_2, RhO_2, MoO_2, IrO_2, Ru, Rh, Pd, Pt, Ir, W, WN, TaN, Os, and OsO_2.

Sub A9

50. A capacitor structure comprising:

a first electrode;

a high dielectric constant material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein at least one of the first and second electrode comprises a diffusion barrier layer formed of $RuSi_xO_y$, where x and y are in the range of about 0.01 to about 10.

51. The structure of claim 50, wherein x and y are in the range of about 0.01 to about 1.

52. The structure of claim 50, wherein the diffusion barrier layer of the first electrode is formed on at least a portion of a silicon containing region and further wherein the structure includes one or more additional conductive layers over the diffusion barrier layer formed of at least one of a metal and a conductive metal oxide.

53. The structure of claim 52, wherein the one or more additional conductive layers are formed from materials selected from the group consisting of RuO_2, RhO_2, MoO_2, IrO_2, Ru, Pt, Ir W, WN, TaN, Os, and OsO_2.

54. A integrated circuit structure comprising:

a substrate assembly including at least one active device and a silicon containing region; and

an interconnect formed relative to the at least one active device and the silicon containing region, the interconnect including a diffusion barrier layer on at least a portion of the silicon containing region, wherein the diffusion barrier layer is formed of $RuSi_xO_y$, where x and y are in the range of about 0.01 to about 10.

55. The structure of claim 54, wherein x and y are in the range of about 0.1 to about 1.

56. The structure of claim 54, wherein x is about 0.4.

57. The structure of claim 54, wherein y is about 0.05.

58. The structure of claim 54, further comprising a conductive contact material formed relative to the diffusion barrier layer.

59. A method for forming a semiconductor device structure having a $RuSi_xO_y$ barrier layer, the method comprising:

(a) placing a semiconductor substrate assembly in a reaction chamber, said semiconductor substrate assembly having a surface;

(b) introducing a ruthenium precursor into said reaction chamber to form a single layer of ruthenium on at least a portion of said semiconductor substrate surface;

(c) introducing a non-reactive gas into said reaction chamber to substantially cover said single layer of ruthenium and purge said ruthenium precursor from said reaction chamber;

(d) introducing a silicon precursor into said reaction chamber to form a single layer of $RuSi_xO_y$ on at least a portion of said semiconductor substrate surface; and

(e) introducing a non-reactive gas into said reaction chamber to substantially cover said single layer of $RuSi_xO_y$ and purge said silicon precursor from said reaction chamber.

60. The method of claim 59, further comprising introducing an oxygen-containing substance into said reaction chamber to form a single barrier layer of $RuSi_xO_y$ on at least a portion of said semiconductor substrate surface.

61. The method of claim 59, wherein introducing a silicon precursor into said reaction chamber comprises introducing a silicon precursor in an oxidizing atmosphere within said reaction chamber.

Sub a10

62. The method of claim 61, wherein introducing a silicon precursor in an oxidizing atmosphere comprises introducing said silicon precursor in an atmosphere comprising air, oxygen, or an oxygen-containing compound.

63. The method of claim 59, wherein said ruthenium precursor comprises $C_6H_8Ru(CO)_3$.

Sub a11

64. The method of claim 59, wherein introducing a non-reactive gas comprises introducing a non-reactive gas selected from the group consisting of nitrogen, argon, neon, and xenon.

65. The method of claim 59, wherein introducing a silicon precursor comprises introducing silane or disilane into said reaction chamber.

66. The method of claim 59, wherein steps (a) through (e) are repeated to form 3 to 5 $RuSi_xO_y$ barrier monolayers.